What is claimed is:

1. A semiconductor device having a semiconductor integrated circuit, the semiconductor device comprising:

internal lines provided separately within the semiconductor integrated circuit and to each of which a different power source potential is applied from an external line provided outside the semiconductor integrated circuit; and

a switch connected between the internal lines.

2. A semiconductor device having a semiconductor integrated circuit, the semiconductor device comprising:

a first internal line and a second internal line provided within the semiconductor integrated circuit;

a first internal terminal, a second internal terminal, a third internal terminal, and a fourth internal terminal provided within the semiconductor integrated circuit;

a first external line and a second external line provided outside the semiconductor integrated circuit;

a first connection for connecting the first external line and the first internal terminal;

a second connection for connecting the first external line and the second internal terminal;

a third connection for connecting the second external line and the third internal terminal;

a fourth connection for connecting the second external line and the fourth internal terminal;

a first switch connected between the first internal terminal and the first internal line;

a second switch connected between the second internal terminal and the first internal line;

a third switch connected between the first internal line and the second internal line;

a fourth switch connected between the third internal terminal and the second internal line; and

a fifth switch connected between the fourth internal terminal and the second internal line.

3. The semiconductor device according to claim 2, wherein the third switch has a function of limiting a current flowing therein to a predetermined amount when the third switch is in a closed state.

4. The semiconductor device according to claim 2, further comprising, within the semiconductor integrated circuit, a switch controlling section for controlling opening and closing of the first to fifth switches.

5. The semiconductor device according to claim 4, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the first internal line and the second internal line.

6. The semiconductor device according to claim 2, wherein:

the second switch comprises a P-channel MOS transistor, and the semiconductor device further comprises an N-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the P-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the P-channel MOS transistor is connected to the first internal line; and

a gate terminal of the N-channel MOS transistor is connected to the second internal terminal, a source terminal of the N-channel MOS transistor is connected to the fourth internal terminal, and a drain terminal of the N-channel MOS transistor is connected to a gate terminal of the P-channel MOS transistor such that the P-channel MOS transistor is caused to be in a conducting state when a predetermined voltage is supplied to the first external line and the second external line.

7. The semiconductor device according to claim 2, wherein:

the fifth switch comprises an N-channel MOS transistor, and the semiconductor device further comprises a P-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the N-channel MOS transistor is connected to the fourth internal terminal, and a drain terminal of the N-channel MOS transistor is connected to the second internal line; and

a gate terminal of the P-channel MOS transistor is connected to the fourth internal terminal, a source terminal of the P-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the P-channel MOS transistor is connected to a gate terminal of the N-channel MOS transistor, such that the N-channel MOS transistor is caused to be in a conducting state when a predetermined voltage is supplied to the first external line and the second external line.

8. A semiconductor device having a semiconductor integrated circuit, the semiconductor device comprising:

an internal line provided within the semiconductor integrated circuit;

a first internal terminal and a second internal terminal provided within the semiconductor integrated circuit;

a first external line provided outside the semiconductor integrated circuit;

a first connection for connecting the first external line and the first internal terminal;

a second connection for connecting the first external line and the second internal terminal;

a first switch connected between the first internal terminal and the internal line;

a second switch connected between the second internal terminal and the internal line; and

a current detecting section for detecting a current flowing in the internal line.

9. The semiconductor device according to claim 8, further comprising, within the semiconductor integrated circuit, a switch controlling section for controlling opening and closing of the first and second switches.

10. The semiconductor device according to claim 9, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the internal line.

11. The semiconductor device according to claim 8, wherein:

the second switch comprises a P-channel MOS transistor, and the semiconductor device further comprises an N-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the P-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the P-channel MOS transistor is connected to the internal line; and

a gate terminal of the N-channel MOS transistor is connected to the second internal terminal, a source terminal of the N-channel MOS transistor is connected to the second external line, and a drain terminal of the N-channel MOS transistor is connected to a gate terminal of the P-channel MOS transistor, such that the P-channel MOS transistor is caused to be in a conducting state when a predetermined voltage is supplied to the first external line and a second external line provided outside the semiconductor integrated circuit.

12. The semiconductor device according to claim 8, wherein:

the second switch comprises an N-channel MOS transistor, and the semiconductor device further comprises a P-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the N-channel MOS transistor is connected to the first external line, and a drain terminal of the N-channel MOS transistor is connected to the internal line; and

a gate terminal of the P-channel MOS transistor is connected to the first external line, a source terminal of the P-channel MOS transistor is connected to the second external line, and a drain terminal of the P-channel

MOS transistor is connected to a gate terminal of the N-channel MOS transistor, such that the N-channel MOS transistor is caused to be in a conducting state when a predetermined voltage is supplied to the first external line and a second external line provided outside the semiconductor integrated circuit.

13. A semiconductor device having a semiconductor integrated circuit, the semiconductor device comprising:

an internal line provided within the semiconductor integrated circuit;

a first internal terminal, a second internal terminal, and a third internal terminal provided within the semiconductor integrated circuit;

a first external line and a second external line provided outside the semiconductor integrated circuit;

a first connection for connecting the first external line and the first internal terminal;

a second connection for connecting the first external line and the second internal terminal;

a third connection for connecting the second external line and the third internal terminal;

a first switch connected between the first internal terminal and the internal line;

a second switch connected between the second internal terminal and the internal line; and

a third switch connected between the third internal terminal and the internal line.

14. The semiconductor device according to claim 13, further comprising, within the semiconductor integrated circuit, a switch controlling section for controlling opening and closing of the first, second and third switches.

15. The semiconductor device according to claim 14, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected

to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the internal line.

16. The semiconductor device according to claim 14, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit; and

a grounding terminal of the switch controlling section is connected to the third internal terminal.

17. The semiconductor device according to claim 14, wherein:

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit, and

a power source terminal of the switch controlling section is connected to the third internal terminal.

18. The semiconductor device according to claim 13, wherein:

the second switch comprises a P-channel MOS transistor, and the semiconductor device further comprises an N-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the P-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the P-channel MOS transistor is connected to the internal line; and

a gate terminal of the N-channel MOS transistor is connected to the second internal terminal, a source terminal of the N-channel MOS transistor is connected to the second external line, and a drain terminal of the N-channel MOS transistor is connected to a gate terminal of the P-channel MOS transistor, such that the P-channel MOS transistor is caused to be in a conducting state when a predetermined voltage is supplied to the first external line and the second external line.

19. The semiconductor device according to claim 13, wherein:

the second switch comprises an N-channel MOS transistor, and the semiconductor device further comprises a P-channel MOS transistor within

the semiconductor integrated circuit;

a source terminal of the N-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the N-channel MOS transistor is connected to the internal line provided within the semiconductor integrated circuit; and

a gate terminal of the P-channel MOS transistor is connected to the second internal terminal, a source terminal of the P-channel MOS transistor is connected to the second external line, and a drain terminal of the P-channel MOS transistor is connected to a gate terminal of the N-channel MOS transistor, such that the N-channel MOS transistor is caused to be in a conducting state when a predetermined voltage is supplied to the first external line and the second external line.

20. A semiconductor device having a semiconductor integrated circuit, the semiconductor device comprising:

a first internal line provided within the semiconductor integrated circuit;

a first internal terminal and a second internal terminal provided within the semiconductor integrated circuit;

a first external line provided outside the semiconductor integrated circuit;

a second external line provided outside the semiconductor integrated circuit and connected to the first internal line;

a first connection for connecting the first external line and the first internal terminal;

a second connection for connecting the first external line and the second internal terminal;

a first switch connected between the first internal terminal and the first internal line; and

a second switch connected between the second internal terminal and the first internal line.

21. The semiconductor device according to claim 20, further comprising, within the semiconductor integrated circuit, a switch controlling section for controlling opening and closing of the first and second switches.

22. The semiconductor device according to claim 21, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the first internal line.

23. The semiconductor device according to claim 21, wherein:

a power source terminal of the switch controlling section is connected to the first internal line; and

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit.

24. The semiconductor device according to claim 21, wherein:

a grounding terminal of the switch controlling section is connected to the first internal line; and

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit.

25. A method for inspecting a semiconductor device comprising: internal lines which are provided separately within the semiconductor integrated circuit and to each of which a different power source potential is applied from an external line provided outside the semiconductor integrated circuit; and a switch connected between the internal lines, which method comprises:

closing the switch, and inspecting a connection state between the external line and an internal terminal provided within the semiconductor integrated circuit.

26. A method for inspecting a semiconductor device comprising: a first internal line and a second internal line provided within a semiconductor integrated circuit; a first internal terminal, a second internal

terminal, a third internal terminal, and a fourth internal terminal provided within the semiconductor integrated circuit; a first external line and a second external line provided outside the semiconductor integrated circuit; a first connection for connecting the first external line and the first internal terminal; a second connection for connecting the first external line and the second internal terminal; a third connection for connecting the second external line and the third internal terminal; a fourth connection for connecting the second external line and the fourth internal terminal; a first switch connected between the first internal terminal and the first internal line; a second switch connected between the second internal terminal and the first internal line; a third switch connected between the first internal line and the second internal line; a fourth switch connected between the third internal terminal and the second internal line; and a fifth switch connected between the fourth internal terminal and the second internal line, which method comprises:

closing the first, third and fourth switches while opening the second and fifth switches;

applying an inspection signal to the first external line and the second external line; and

inspecting a connection state between the first external line and the first internal terminal at the first connection, and a connection state between the second external line and the third internal terminal at the third connection.

27. The method according to claim 26, wherein the third switch has a function of limiting a current flowing therein to a predetermined amount when the third switch is in a closed state.

28. The method according to claim 26, wherein the semiconductor device comprises, within the semiconductor integrated circuit, a switch controlling section for controlling opening and closing of the first to fifth switches.

29. The method according to claim 28, wherein

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the first internal line and the second internal line.

30. The method according to claim 26, wherein:

the second switch comprises a P-channel MOS transistor, and the semiconductor device further comprises an N-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the P-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the P-channel MOS transistor is connected to the first internal line;

a gate terminal of the N-channel MOS transistor is connected to the second internal terminal, a source terminal of the N-channel MOS transistor is connected to the fourth internal terminal, and a drain terminal of the N-channel MOS transistor is connected to a gate terminal of the P-channel MOS transistor; and

the P-channel MOS transistor is caused to be in a conducting state by supplying a predetermined voltage to the first external line and the second external line.

31. The method according to claim 26, wherein:

the fifth switch comprises an N-channel MOS transistor, and the semiconductor device further comprises a P-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the N-channel MOS transistor is connected to the fourth internal terminal, and a drain terminal of the N-channel MOS transistor is connected to the second internal line;

a gate terminal of the P-channel MOS transistor is connected to the fourth internal terminal, a source terminal of the P-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the P-channel MOS transistor is connected to a gate terminal of the N-channel MOS transistor; and

the N-channel MOS transistor is caused to be in a conducting state by supplying a predetermined voltage to the first external line and the

second external line.

32. A method for inspecting a semiconductor device comprising: an internal line provided within the semiconductor integrated circuit; a first internal terminal and a second internal terminal provided within the semiconductor integrated circuit; a first external line provided outside the semiconductor integrated circuit; a first connection for connecting the first external line and the first internal terminal; a second connection for connecting the first external line and the second internal terminal; a first switch connected between the first internal terminal and the internal line; a second switch connected between the second internal terminal and the internal line; and a current detecting section for detecting a current flowing in the internal line, which method comprises:

closing the first switch while opening the second switch; and

inspecting a connection state between the first external line and the first internal terminal at the first connection according to a detection result by the current detecting section.

33. The method according to claim 32, wherein the semiconductor device comprises, within the semiconductor integrated circuit, a switch controlling section for controlling opening and closing of the first and second switches.

34. The method according to claim 33, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the internal line.

35. The method according to claim 32, wherein:

the second switch comprises a P-channel MOS transistor, and the semiconductor device further comprises an N-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the P-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the P-channel MOS transistor is connected to the internal line;

a gate terminal of the N-channel MOS transistor is connected to the second internal terminal, a source terminal of the N-channel MOS transistor is connected to the second external line, and a drain terminal of the N-channel MOS transistor is connected to a gate terminal of the P-channel MOS transistor; and

the P-channel MOS transistor is caused to be in a conducting state by supplying a predetermined voltage to the first external line and a second external line provided outside the semiconductor integrated circuit.

36. The method according to claim 32, wherein:

the second switch comprises an N-channel MOS transistor, and the semiconductor device further comprises a P-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the N-channel MOS transistor is connected to the first external line, and a drain terminal of the N-channel MOS transistor is connected to the internal line;

a gate terminal of the P-channel MOS transistor is connected to the first external line, a source terminal of the P-channel MOS transistor is connected to the second external line, and

a drain terminal of the P-channel MOS transistor is connected to a gate terminal of the N-channel MOS transistor; and the N-channel MOS transistor is caused to be in a conducting state by supplying a predetermined voltage to the first external line and a second external line provided outside the semiconductor integrated circuit.

37. A method for inspecting a semiconductor device comprising: an internal line provided within the semiconductor integrated circuit; a first internal terminal, a second internal terminal, and a third internal terminal provided within the semiconductor integrated circuit; a first external line and a second external line provided outside the semiconductor integrated circuit; a first connection for connecting the first external line and the first internal terminal; a second connection for connecting the first external line and the second internal terminal; a third connection for connecting the second external line and the third internal terminal; a first switch

connected between the first internal terminal and the internal line; a second switch connected between the second internal terminal and the internal line; and a third switch connected between the third internal terminal and the internal line, which method comprises:

closing the first and third switches while opening the second switch; and

inspecting a connection state between the first external line and the first internal terminal at the first connection.

38. The method according to claim 37, wherein the semiconductor device comprises, within the semiconductor integrated circuit, a switch controlling section for controlling opening and closing of the first, second and third switches.

39. The method according to claim 38, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the internal line.

40. The method according to claim 38, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit; and

a grounding terminal of the switch controlling section is connected to the third internal terminal.

41. The method according to claim 38, wherein:

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

a power source terminal of the switch controlling section is connected to the third internal terminal.

42. The method according to claim 37, wherein:

the second switch comprises a P-channel MOS transistor, and the semiconductor device further comprises an N-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the P-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the P-channel MOS transistor is connected to the internal line;

a gate terminal of the N-channel MOS transistor is connected to the second internal terminal, a source terminal of the N-channel MOS transistor is connected to the second external line, and a drain terminal of the N-channel MOS transistor is connected to a gate terminal of the P-channel MOS transistor; and

the P-channel MOS transistor is caused to be in a conducting state by supplying a predetermined voltage to the first external line and the second external line.

43. The method according to claim 37, wherein:

the second switch comprises an N-channel MOS transistor, and the semiconductor device further comprises a P-channel MOS transistor within the semiconductor integrated circuit;

a source terminal of the N-channel MOS transistor is connected to the second internal terminal, and a drain terminal of the N-channel MOS transistor is connected to the internal line provided within the semiconductor integrated circuit;

a gate terminal of the P-channel MOS transistor is connected to the second internal terminal, a source terminal of the P-channel MOS transistor is connected to the second external line, and a drain terminal of the P-channel MOS transistor is connected to a gate terminal of the N-channel MOS transistor; and

the N-channel MOS transistor is caused to be in a conducting state by supplying a predetermined voltage to the first external line and the second external line.

44. A method for inspecting a semiconductor device comprising: a first internal line provided within the semiconductor integrated circuit; a first internal terminal and a second internal terminal provided within the

semiconductor integrated circuit; a first external line provided outside the semiconductor integrated circuit; a second external line provided outside the semiconductor integrated circuit and connected to the first internal line; a first connection for connecting the first external line and the first internal terminal; a second connection for connecting the first external line and the second internal terminal; a first switch connected between the first internal terminal and the first internal line; and a second switch connected between the second internal terminal and the first internal line, which method comprises:

closing the first switch while opening the second switch;

applying an inspection signal from the first external line to the second external line; and

inspecting a connection state between the first external line and the first internal terminal at the first connection.

45. The method according to claim 44, wherein the semiconductor device comprises, within the semiconductor integrated circuit, a switch controlling section for controlling opening and closing of the first and second switches.

46. The method according to claim 45, wherein:

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit;

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit; and

at least one of the internal power source line and the internal grounding line is separated from the first internal line.

47. The method according to claim 45, wherein:

a power source terminal of the switch controlling section is connected to the first internal line; and

a grounding terminal of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside the semiconductor integrated circuit.

48. The method according to claim 45, wherein:

a grounding terminal of the switch controlling section is connected to the first internal line; and

a power source terminal of the switch controlling section is connected to an internal power source line connected to a power source line provided outside the semiconductor integrated circuit.